

Japanese Unexamined Patent Application S58-102394

(19)Japan Patent Office (JP)

(11)Japanese Patent Application Publication

Japanese Unexamined Patent Application Publication (A)

S58-102394

(51)Int. Cl.³ Identification Number JPO File Number (43)Publication June 17, 1983
 G 11 C 27/00 7343-5B

Number of Inventions: 1

Request for Examination Not Yet Requested

(Total of 4 Pages)

(54)Title of the Invention Memory Devices

(21)Japanese Patent Application S56-201933

(22)Application December 15, 1981

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Specification

1. Title of the Invention

Memory Devices

2. Detailed Explanation of the Invention

Memory devices continuously storing multiple pieces of analog data information,
 in which required number of MIS transistors with non-volatile memory functions that

are electronically re-writable are placed in parallel; all drain ends are open ends, all gate ends are mutually short-circuited, and source ends are dependent on its own transistor but not each other; by giving a certain voltage to the gate ends and by giving the sources voltages different each other; by changing threshold voltages of the abovementioned MIS transistors by voltage differences between the gates and the sources, analog data information entering from source ends is stored.

3. Detailed Explanation of the Invention

This invention is related to memory devices that continuously store multiple pieces of analog data information.

Conventionally, in order to store multiple pieces of analog data information, the so-called memory array is used. For this memory, there are several kinds including semi-conductor memory. By the way, to store analog information, usually, analog information is converted into digital information at first by an A / D converter, which is then stored in a memory array. Therefore, in order to store multiple pieces of analog information, A / D converters and a memory array equivalent to the bits of converted digital information are required. In particular, when this analog information is input continuously at a high speed, rapid A / D conversion becomes necessary; when extremely rapid conversion is required, sometimes the only possible way is the conversion done by the use of multiple A / D converters that work rapidly placed in parallel. What is particularly troublesome is that after digital information, which has been once A / D converted as mentioned above, is stored, the original analog information is required upon reading of data. For example, like video signals and audio signals, when analog information needs to be stored at a certain level of high speed continuously, to meet this requirement, a somewhat complicated system, which is also wasteful, is necessary.

In this invention, these problems are solved; first, devices in which analog information is stored are to be provided; second, simple and useful systems in which information is stored continuously at a high speed are to be provided.

The following is the detailed explanation accompanied with the figures.

In Figure 1, a P-channel MIS transistor with the MNOS structure is shown as an example of non-volatile memory that is electronically re-writable. Being P channel is solely for the purpose of explanation and N channel works as well. In the figure, D, S, G, and B refer to a drain, a source, a gate and a circuit board, respectively. 1 is made from a very thin oxide film, and 2 is made from a nitride film. If, for example, with the drain and the source kept open, a sufficiently great voltage difference, which is positive against the circuit board of B, is applied to the gate of G, electrons are poured from the circuit board in the insulated film indicated by the very thin oxide film of 1 and the nitride film of 2 in Figure 1, and as a result a threshold voltage of V_{th} of this MIS transistor shifts to a positive value. On the contrary, if a sufficiently great voltage difference, which is negative against the circuit board of B, is applied to the gate, the electrons that have been poured from these are again released to the circuit board and V_{th} shifts to the negative side. This is the operating principle of the conventional MNOS memory. It is apparent from the explanation above that pouring and releasing of electrons depend only on the circuit board of B and the gate of G. What effects do the drain and source have? In general, a drain and a source are used in an open manner. However, here, in the following section, is explained a case where a voltage is applied in the PN junction reverse-biased direction against the circuit board. Moreover, it should be mentioned that a drain and a source are interchangeable; therefore either will do. Here is described the case in which a source and a circuit board are PN junction reverse biased. The same is true for a drain and for a case in which a voltage is applied to both of a source and a drain at the same time.

- (1) When electrons are poured, there is almost no effect.
- (2) When electrons are released, to make the same V_{th} change, VGS, i.e., the same amount of voltage difference between the gate and the source is necessary. For example, the source and the circuit board are short-circuited, and to shift V_{th} by -1 V, -30 V between the gate and the circuit board is required; then, when -5 V between the source and the circuit board is applied, in order to shift V_{th} by -1 V, -35 V is necessary between the gate and the circuit board. Therefore, this means

that a change in V_{th} depends on VGS. This is shown in Figure 2. According to the experiments, a V_{th} change can be divided in three parts: in Figure 2, the part (a) is the part where V_{th} does not change although VSG changes; the part (b) is the part where V_{th} changes exponentially as VSG changes; the part (c) is the part where V_{th} reached to saturation and V_{th} does not change anymore. It is needless say that in general the part (c) is used. In this invention, the part (b) in Figure 2 is used. That is to say, in this part, V_{th} changes in an analog manner with VSG and it is easy to make fine adjustments of V_{th} , because the change is exponential, which is preferable.

The phenomenon shown in Figure 2 appears to arise from a vacuum layer caused by reverse-biased PN junction, resulting in suppression of electron release. Conventionally, when sufficiently great reverse bias is added upon selection of memory source, suppression of electron release has been observed (equivalent to the part of (a) in Figure 2), and it has been known that illumination prevents electron release even with a drain and a source opened; all these are said to be due to the existence of a vacuum layer, which is consistent with our explanation above. Consequently, this phenomenon will bring about the exactly same effects not only on the MNOS structure but also on floating gate memory and avalanche memory, when electrons are released.

Moreover, characteristics in Figure 2 are different from convention and novel in that: what has been assumed about conditions between a circuit board and a gate in the past is clarified in terms of conditions between a gate and a source: as will be mentioned later, this operating principle is made extremely usable in integrated circuits: and the part of (b) in Figure 2, which has been ignored, is used for analog memory functions.

In Figure 3, one embodiment of the memory devices in this invention is shown. In Figure 3, the transistors in parallel, referred to as 3, are memory that is non-volatile and electronically re-writable, as already mentioned; the circuit board is shared and is connected at the maximum voltage (in P channels like the sturcture in Figure 1 and integrated circuits), and all gates are short-circuited and connected to

the GATE terminals as shown in Figure 3. In these transistors, to the source of S and the drains of D, electric switches of 4 and 6 are connected respectively. These electric switches are realized with MOS transistors and the like with ease. The switches of 4 at the source end and the switches of 6 at the drain end work differently. The other ends of the switches of 4 at the end of the source are all short-circuited to become the DATA terminals.

Here is an example to show how analog information is continuously input to the DATA terminals and analog information is stored at the transistors of 3 at a high speed and continuously. To attain this, first, all of the switches of the drain end of 6 are opened. Second, to the DATA terminals, a certain sufficient voltage that is negative against the circuit board is applied (when the transistors of 3 are P channels, and this condition also applies to the rest of this example). Next, to the DATA terminals, continuous analog information is sent without conversion and at the same time this continuous analog information (measured by duration) is divided into certain smaller portions by duration and stored; at the phase that is equivalent to the minimum duration at the time the data are divided by duration, the switches at the source end of 6 are closed one after another and are opened again. By doing this, analog information that is input continuously is placed to the transistors of 3 at their source sides from the left to the right one after another as time passes. Because the voltage at the GATE terminals remains always constant, transient VSG depends on each transistor, and accordingly V_{th} varies, which is stored in the transistors of 3.

Here, how this stored analog information is retrieved is shown. This time, a certain voltage is placed on the DATA terminals, all the switches of 6 are closed, and the voltage required for retrieval is placed on the GATE terminals. When all data are needed, all of the switches of 4 can be closed at the same time; when data are needed sequentially, switches can be closed at such a phase one after another. By setting the GATE terminals in a certain way, from the DATA terminals, electric current equivalent to the V_{th} difference of each transistor flows into each OUT terminal.

On the basis of this invention, continuous input of analog information is easy and

because output is in an analog manner, there is no need to convert from A to D and again from D to A. As a result, this is notably simple and useful.

4. Brief Description of the Drawings

Figure 1 illustrates the structure of conventional MNOS memory. Figure 2 is the plot of electron release in conventional MNOS memory. Figure 3 illustrates the schematic circuit diagram of a memory device, one embodiment of this invention.

1. the extremely thin oxide film
2. the nitride film
3. MNOS transistors
4. and 6. switches

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[Japanese Unexamined Patent Application S58-102394(3) contains Figures 1 and 2.]

[Japanese Unexamined Patent Application S58-102394(4) contains Figure 3.]

⑫ 公開特許公報 (A)

昭58—102394

⑤ Int. Cl.³
G 11 C 27/00

識別記号

庁内整理番号
7343—5B

⑬ 公開 昭和58年(1983)6月17日

発明の数 1
審査請求 未請求

(全 4 頁)

⑭ 記憶装置

⑰ 特 願 昭56—201933

⑱ 出 願 昭56(1981)12月15日

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明 細 書

1. 発明の名称

記憶装置

2. 特許請求の範囲

複数個のアナログデータ量を連続して記憶する装置において、電気的に書きかえ可能な不揮発性メモリ作用をもつ MIS 型トランジスタを必要な複数個並列に配置し、ドレイン端はすべて開放とし、ゲート端は各トランジスタにそれぞれ独立の電圧を加え、ゲート端に所定の電圧を加え、ソースにはそれぞれ異なる電圧を加えて、ゲート・ソース間の電位差により前記 MIS 型トランジスタのスレシヨルド電圧を変化させることにより、ソース端に入つてアナログデータ量を記憶することを特徴とする記憶装置。

3. 発明の詳細な説明

本発明は複数個のアナログデータ量を連続して記憶する記憶装置に関するものである。

従来複数個のデータを記憶するにはいわゆるメ

モリアレイを用いている。このメモリには半導体メモリを始め各種のものがある。ところでアナログ量を記憶するのは一旦 A/D 変換器によりアナログ量をデジタル量に変換し、そしてメモリアレイに記憶するのが常である。従つて複数個のアナログ量を記憶するには A/D 変換器と、デジタル変換されたビット数に相当するメモリアレイが必要となる。特にこのアナログ量が高速に連続して入力される時には高速 A/D 変換が必要となり、最高速を要求される時には並列に高速 A/D 変換器を複数個並べて処理するしか方法がないこともある。特に問題なのは一旦この様に A/D 変換を行つてデジタル量で記憶していても、読み出す時は又元のアナログ量が欲しいという時である。例えばビデオ信号やオーディオ信号の様に、ある程度高速で連続してアナログ量を記憶しなければならない時に、これらの要求にこたえるには可成の複雑でかつムダなシステムが必要となる。

本発明はこれらの欠点を除去し、まずアナログ量を記憶するデバイスを提供し、ついで高速連続

記憶の為の簡単で有能なシステムを提供せんとするものである。

以下図面を参照しながら詳細に説明する。

第1図は電氣的に書きかえ可能な不揮発性メモリの一例としてMNO S構造のPチャネルMIS型トランジスタを示した。Pチャネルであることは説明の都合の為でありNチャネルであつても同様である。図中D、S、G、Bはそれぞれドレイン、ソース、ゲート、基板であり、1はごく薄い酸化膜、2は窒化膜である。今ドレイン、ソースを開放端のまま基板Bに対し十分に大きいプラス電位差をゲートGに印加すると、基板より電子が第1図のごく薄い酸化膜1、窒化膜2で示された絶縁膜に注入され、このMISトランジスタのスレシヨルド電圧 V_{th} は正へ移動する。逆に基板Bに対し十分に大きいマイナス電位差をゲートGにかけると、これら注入された電子は再び基板へ放出され V_{th} は負側へ移動する。これが一般的なMNO Sメモリの動作原理である。以上の説明から明らかなごとく、電子の注入、放出には基板B

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の領域に分けられ第2図で(a)の領域は V_{GS} を変化させても V_{th} 変化がない領域、(b)の領域は V_{GS} を変えると指数関数的に V_{th} 変化がある領域(c)の領域は V_{th} 変化が飽和に達し、もはや変化がなくなる領域である。一般には(c)の領域を用いていることはいうまでもない。本発明は第2図の(b)の領域を用いる。つまりこの領域では V_{GS} により V_{th} 変化がアナログ的に変化し、都合のよいことに指数関数的変化のため V_{th} のこまかい変化を調整することも容易である。

第2図に示す現象は、PN接合の逆バイアスにより空乏層が生じ、これが電子放出を妨げているものと思われる。従来でもメモリのソース選択において十分に大きな逆バイアスを加えると電子放出がおきないこと(第2図の(a)の領域に当たる)や光を当てるとドレイン、ソース開放でも電子放出がおこらないこと等が知られておりこれらがいづれも空乏層の存在によるものと言われていることと一致する。従つてこの現象はMNO S構造のみならずフローティングゲート型やアバランシェ型

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とゲートGのみが関与している。ドレイン、ソースはどの様な影響を及ぼすのであろうか。一般にはドレイン、ソースは開放で用いるが、今これらを基板に対しPN接合逆バイアスする方向へ電圧を加えていつた結果をまとめると次の様になる。但しドレインとソースは完全に交換可能であるから、いづれか一方、今の場合ソースと基板にPN接合逆バイアスをかけた場合について述べる。ドレインについても、又ソース、ドレイン双方に同時に電圧を印加した時も同様である。

- (1) 電子注入の場合はほぼ影響なし。
- (2) 電子放出の場合は、同一の V_{th} 変化をきたすためには V_{GS} つまりゲートとソース間の電位差が同じ量必要である。例えばソースと基板短路して、 V_{th} を-1V移動さすのにゲート、基板間は-30V必要であつたとすると、ソース、基板間に-5Vかけた時に V_{th} を-1V移動さすには、ゲート、基板間に-35V必要になる。つまりこの事は、 V_{th} 変化は V_{GS} で決まることになる。この模様を第2図に示した。実験によると、 V_{th} 変化は3つ

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のメモリにおいても、電子放出を行う際に全く同様の効果を示すことになる。

又、第2図の特性が従来と異なり新規性のある点は、従来基板、ゲート間について推測的に知られていたことを、ゲート、ソース間について明らかにして、後述のごとく集積回路内できわめてこの動作を利用しやすくしたことにあることと、従来かえりみられなかつた第2図の(b)の領域をアナログ記憶作用として用いる所にある。

第3図に本発明の記憶装置の一実施例を示す。第3図に於て、トランジスタ並列群3は既に述べた電氣的書きかえ可能な不揮発性メモリで、基板は共通でこの回路の最高電位(第1図の構造のようにPチャネルの場合、かつ集積回路の場合)に、ゲートは第3図に示すごとくすべて短絡してGATE端子に接続してある。このトランジスタのソースS及びドレインDにはそれぞれ電氣的スイッチ群4、6が接続されている。この電氣的スイッチはMOSトランジスタ等で容易に実現できる。ソース端のスイッチ群4とドレイン端のスイッチ群6

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はその作用が異なる。ソース端Sのスイッチ群4の
もう一端はすべて短絡してDATA端子となし
てある。

今アナログ量がDATA端子に連続して入力さ
れた場合、トランジスタ群3に高速に連続的にア
ナログ量が記憶されることを示そう。この為には
まずドレイン端のスイッチ群6をすべて開放にす
る。次にGATE端子を基板に対して所定の十分
な量のマイナス電位差（但しトランジスタ3はド
チャネルの時。以下同じ）をかけ、次にDATA
端子に連続したアナログ量をそのまま流すと同時
にこのアナログ連続量（時間について）を適当に
時分割して記憶する訳だが、その時分割の最小分
割時間の位相をもつて、ソース端のスイッチ群6
を順次閉じて又開いてゆく。こうすれば、連続し
て入力したアナログ量が時間の経過と共に、トラ
ンジスタ群3のソース端へ左から右へ順次印加さ
れることになる。ここでGATE端子は常に一定
電位の為、経過VGSが各トランジスタに対して異
なり、それに応じた V_{th} 変化がトランジスタ群3

に記憶されることになる。

次にこの記憶されたアナログ量を読み出すこと
を示す。この時にはDATA端子に一定電位をか
け、スイッチ群6はすべて閉じて、GATE端子
は読み出しに必要な電圧に設定すればよい。一斉
に全データが欲しい時はスイッチ群4を全部一斉
に閉じればよいし、順次データが欲しい時はスイ
ッチ群をそのような位相で順次閉じてやればよい。適
当なGATE端子の設定によりDATA端子より
各トランジスタの V_{th} 差に相当する電流がOUT
と示した各端子に現れることになる。

本発明によると、アナログ量が時間的に連続に
入力することは容易であり、又アナログ量で出力
される為 $A/D \rightarrow D/A$ といった二度の変換作用も不
要できわめて簡単で有用であることがわかる。

4. 図面の簡単な説明

第1図は一般のM N O Sメモリの構造を示す図。
第2図は一般のM N O Sメモリの電子放出の時
の特性図。第3図は本発明の一実施例を示す記憶
装置の回路図である。

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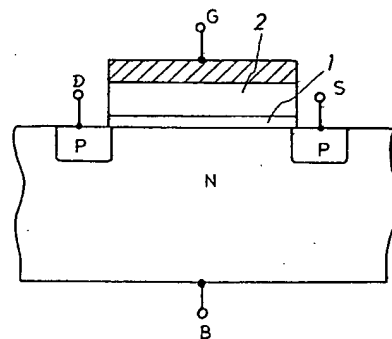
- 1 ... 極薄酸化膜 2 ... 窒化膜
3 ... M N O S トランジスタ群
4、6 ... スイッチ群

特許出願人 シチズン時計株式会社

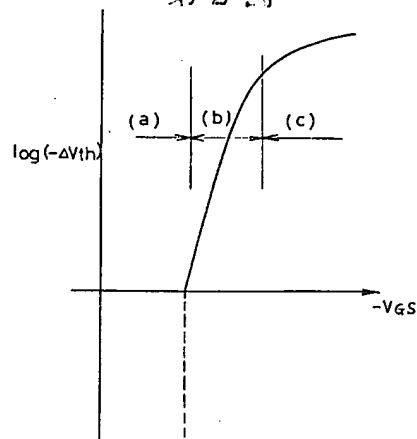


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第1図

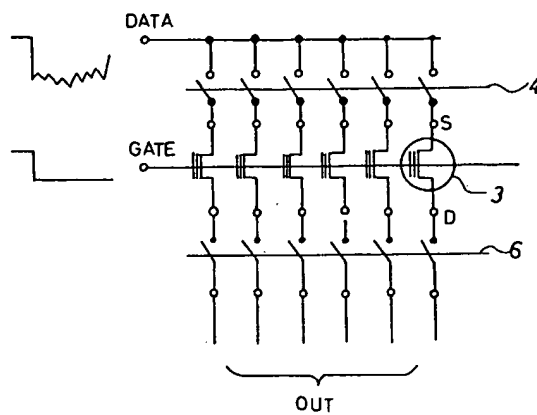


第2図



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第3圖



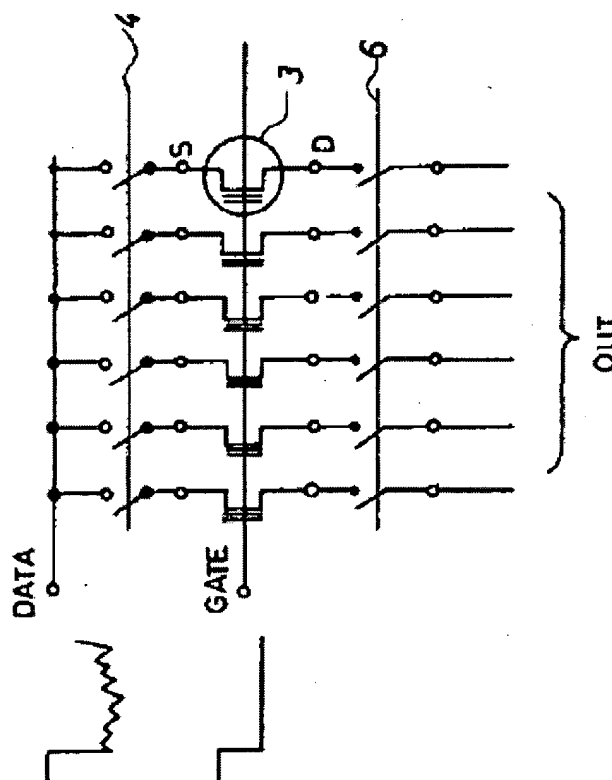
STORAGE DEVICE

Patent number: JP58102394
Publication date: 1983-06-17
Inventor: HASHIMOTO SHINGO; others: 01
Applicant: CITIZEN TOKEI KK
Classification:
- international: G11C27/00
- european:
Application number: JP19810201933 19811215
Priority number(s):

Abstract of JP58102394

PURPOSE: To store plural analog data successively by using an area where its threshold voltage varies according to an exponential function when VGS of characteristic during the electron emission of an MNOS memory is varied as an analog storage operating area.

CONSTITUTION: In storing plural analog data successively, an area where the threshold voltage of an MIS type FET varies according to an exponential function varies when the potential difference VGS between the gate and source with regard to characteristics of an MNOS memory during electron emission is utilized as an analog memory. A switch group 6 at source terminal of this MIS type FET group 3 is opened and a terminal DATA is applied with a successive analog signal while a terminal GATE is held at a potential much less than the substrate; and the switch group 6 is closed successively and then opened to store said analog signal in the FET group 3 successively. Thus, analog information is inputted successively with time.



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